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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,667	06/05/2006	Taichi Majima	0670-7075	4570

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EXAMINER
YU, LIHONG

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

		Application No.	Applicant(s)
Office Action Summary		10/581,667	MAJIMA, TAICHI
		Examiner	Art Unit
		LIHONG YU	2611

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2010*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-24* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some * c)☐ None of:

        1.☒ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

U.S. Patent and Trademark Office

PTOL-326 (Rev. 08-06)   **Office Action Summary**   Part of Paper No./Mail Date 20100301

DETAILED ACTION

Response to Arguments

1.   Applicant's amendment to the claim, received on January 04, 2010, with respect to the

double patenting rejection in the office action on September 01, 2009, has been fully considered

and is persuasive. The nonstatutory obviousness-type Double Patenting rejection of claim 6 has

been withdrawn.

2.   Applicant's arguments with respect to claim rejections under 35 U.S.C. 102 and 103 have

been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3.   Claim 18 is objected to because of the following informalities:

        Claim 18, line 2, **"protected to the redundant bit addition unit"** is not clear in

meaning. For examination purposes, it is interpreted as "provided to the redundant bit addition

unit". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

        The specification shall contain a written description of the invention, and of the manner and process of making
        and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode
contemplated by the inventor of carrying out his invention.

5.   Claims 13, 20, 23 and 24 are rejected under 35 U.S.C. 112, first paragraph, as failing to

comply with the written description requirement. The above independent claims contain subject

matter which was not described in the specification in such a way as to reasonably convey to one

skilled in the relevant art that the inventor(s), at the time the application was filed, had

possession of the claimed invention. Specifically, claims 13, 20, 23 and 24 recite "wherein the

redundant bit unit operates to select as a redundant bit to be added a bit being common to both

symbol data located at a positive position and symbol data located at a negative position out of

the Gray coded 4-level symbols, the positive position and the negative position being away in

deviation furthest from each other", which is not disclosed in the original application, therefore,

it is considered a new matter.

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
such that the subject matter as a whole would have been obvious at the time the invention was made to a person
having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
manner in which the invention was made.

7.   Claims 13-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al

(US 5,214,656) in view of Tanaka et al (US 5,677,681) and Vermesse (US 4,984,191).

Consider claims 13, 20, 23 and 24:

Chung discloses a transmission device (*see Chung at Fig. 1 and col. 2, lines 30-33, where Chung describes a transmitter embodiment of an invention; see Fig. 2 and col. 5, lines 27-47, where Chung describes a corresponding receiver that performs the inverse function of the transmitter*) comprising:

- a redundant bit addition unit for adding a redundant bit of one bit to each of specific bits to be protected to generate coded data, the specific bits being selected out of supplied data (*see Chung at Fig. 1 and col. 4, lines 10-36, where Chung describes that the more important data of the received data is input to channel encoder 121 which adds redundant bits r1 to the data bits m1 to generate m1+r1 data bits, since m1 is number of data bits and r1 is number of redundant bits, m1 might be 1 and r1 might be 1, as is shown at Fig. 5, constellation (A)*); and

- a modulation unit for generating a modulation wave signal by modulating symbol data in accordance to a Gray code sequence (*see Chung at col. 4, lines 37-68, where Chung describes that the coded output from the channel encoder 121 is provided to modulator 150; see Chung at col. 2, lines 20-28, where Chung describes quaternary amplitude modulation (QAM); see Fig. 5, constellation (A), where Chung shows that any pairs of nearest-neighbor symbols in the constellation differ in only a single bit position, that is, Gray code*), the symbol data being obtained as a unit of 2 bits consisting of each bit and its redundant bit for the specific bits to be protected and a unit of 2 bits for the other data bits, on the basis of the coded data generated by the redundant bit addition unit, to send the generated modulated wave signal (*see Chung at Fig. 1 and col. 4, lines 10-36, where Chung describes that the encoded more*

> *important data (m1+r1) and less important data (m2+r2) are provided to a*
>
> *multiplexer 140, when m1=1, m2 =1 and r1 =1, r2 =1),*

However, Chung does not specifically disclose (1), the above modulation is 4-value FSK, and (2), selecting as a redundant bit to be added a bit being common to both symbol data located at a positive position and symbol data located at a negative position out of the symbols, the positive position and the negative position being away in deviation furthest from each other.

Regarding (1) above, Tanaka teaches a 4-value FSK (*see Tanaka at Fig. 3B, Fig. 7 and col. 9, lines 15-36, where Tada describes a 4-value FSK modulation in which quaternary signals '00', '01', '11' and '10' is used*).

It would have been obvious to one skilled in the art at the time the invention was made to modify the invention of Thapar, and to have multi-valued FSK, as taught by Tanaka, thus allowing for reduction in size and power consumption, as discussed by Tanaka (*see Tanaka at col. 3, lines 16-25*).

Regarding (2) above, Vermesse teaches selecting as a redundant bit to be added a bit being common to both symbol data located at a positive position and symbol data located at a negative position out of the symbols, the positive position and the negative position being away in deviation furthest from each other (*see Vermesse at the Abstract, where Vermesse describes selecting a redundant bit which is common both to the more significant bits and the less significant bits*).

It would have been obvious to one skilled in the art at the time the invention was made to modify the invention of Chung, and to select as a redundant bit to be added a bit being common

to both symbol data located at a positive position and symbol data located at a negative position

out of the symbols, as taught by Vermesse, thus making detecting the last recorded value easy

and quick, as discussed by Vermesse (*see Vermesse at col. 1, lines 19-26*).

Consider claim 14:

Chung in view of Tanaka and Vermesse discloses the transmission device according to

claim 13 above. Chung discloses each of the specific bits to be protected comprises flag data (*see*

Chung at col. 6, lines 25-52, where Chung describes that each subset of data has an identifier

that is a two bit pattern).

Consider claim 15:

Chung in view of Tanaka and Vermesse discloses the transmission device according to

claim 13 above. Although Chung does not specifically disclose the supplied data includes bits for

error check and the specific bits to be protected include the bits for error check., it would have

been obvious to one skilled in the art at the time the invention was made to modify the invention

of Chung, and to include bits for error check, as is known in the art to help correct bit errors.

Consider claim 16:

Chung in view of Tanaka and Vermesse discloses the transmission device according to

claim 13 above. Chung does not specifically disclose the supplied data includes bits for error

correction and the specific bits to be protected include the bits for error correction.

It would have been obvious to one skilled in the art at the time the invention was made to modify the invention of Chung, and to include bits for error correction, as is known in the art to improve data quality.

Consider claim 17:

Chung in view of Tanaka and Vermesse discloses the transmission device according to claim 13 above. Chung discloses the number of the specific bits to be protected is less than the number of the other bits not to be protected (*see Chung at Fig. 5 and col. 6, lines 1-15, where Chung discloses the percentage of more important data varying from 37.5% to 62.5%*).

Consider claim 18:

Chung in view of Tanaka and Vermesse discloses the transmission device according to claim 13 above. Chung discloses the data provided to the redundant bit addition unit is data whose high and low significant levels are predetermined and the redundant bit addition unit operates to add the redundant bits to data having a higher significant level (*see Chung at Fig. 1 and col. 4, lines 10-36, where Chung describes that the more important data of the received data is input to channel encoder 121 which adds redundant bits r1 to the data bits for error protection*).

Consider claim 19:

Chung in view of Tanaka and Vermesse discloses the transmission device according to claim 13 above. Chung discloses the supplied data represents a plurality of pieces of information, and the redundant bit addition unit operates for respective ones of the plurality of pieces of

information to add the redundant bit data to each of the specific bits to be protected to generate

the coded data (*see Chung at col. 4, lines 10-36, where Chung describes that the more important*

data of the received data is input to channel encoder 121 which adds redundant bits r1 to the

data bits m1 to generate m1+r1 data bits, since m1 is number of data bits and r1 is number of

redundant bits, m1 might be 1 and r1 might be 1).

Consider claim 21:

Chung in view of Tanaka and Vermesse discloses the reception device according to claim

20 above. Chung discloses the demodulation unit demodulates the received signal by converting

the received signal into a signal of a voltage corresponding to a frequency of the received signal,

and the symbol decision unit performs the symbol decision by comparing the voltage of the

signal, which has been demodulated by the demodulation unit, with preset threshold values (*see*

Chung at Fig. 2 and col. 5, lines 27-47, where Chung describes demodulator 350 and decoders

331, 332 and 310).

Consider claim 22:

Chung in view of Tanaka and Vermesse discloses the reception device according to claim

20 above. Chung discloses the bit data generated by the bit conversion unit is data in which bits

are arranged such that high and low of significance levels thereof are predetermined and the bit

data having the high significance level is added with the redundant bit, and wherein the data

recovery unit deletes the redundant bit added to the bit data having the high significance level

(*see Chung at col. 5, lines 40-47, where Chung discloses that the decoder provides the inverse*

function of the encoder of the transmitter to provide the received signal).

Conclusion

8.   Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to LIHONG YU whose telephone number is (571) 270-5147. The

examiner can normally be reached on 8:30 am-7:00 pm Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Shuwang Liu can be reached on (571) 272-3036. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lihong Yu/
Examiner, Art Unit 2611
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611